



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

in patent application of

Applicant: Udayakumar et al.  
Application No.: 10/620,516  
Filed: July 16, 2003  
For: HYDROGEN BARRIER FOR PROTECTING FERROELECTRIC  
CAPACITORS IN A SEMICONDUCTOR DEVICE AND METHODS  
FOR FABRICATING THE SAME

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

1. Pursuant to 37 C.F.R. 1.97 and 1.98, and in compliance with 37 C.F.R. 1.56, the Office's attention is directed to the patents, pending applications, publications and other information listed on the attached PTO-1449. A copy of each listed document is enclosed except for: (a) pending applications or (b) those previously cited or submitted to the Office in the following application(s) upon which this application relies for an earlier filing date under 35 U.S.C. 120:

Serial No.: \_\_\_\_\_  
Filing Date: \_\_\_\_\_

Regarding any document, publication or other information for which a date is not given on the attached PTO-1449, Applicant(s) believe(s) the same may qualify as "prior" art to this application and should be treated accordingly, although Applicant(s) reserve(s) the right to contest the prior art status of any document, publication or information, should issue arise.

2. Regarding each listed document that is not in the English language, an English-language translation accompanies this Statement as indicated on the attached PTO-1449 or a concise explanation of the relevance of the document is set forth in the following document(s):

- (a) ☐ Copy of each English language version of a search report indicating the degree of relevance found by the foreign office of each document being submitted from the search report.
- (b) ☐ Attachment entitled "Concise Explanation of Relevance of Non-English Language Documents".

3. Pursuant to 37 C.F.R. 1.97(b) this Statement is being filed (one must be checked):

- (a) ☒ Within 3 months of the filing date or date of entry into the National Stage.
- (b) ☐ Before the mailing date of a first Office Action on the merits. If this Statement is not filed before the mailing date of a first Office Action on the merits, the required certification is given below or, in the absence thereof, the Office is authorized to charge the required fee set forth in 37 C.F.R. 1.17(p) to Deposit Account No. 20-0668 for consideration of this Statement.
- (c) ☐ Before the mailing date of a first Office Action on the merits after a first or second submission under 37 C.F.R. 1.129(a).

(d) \_\_\_ After the period set forth in 37 C.F.R. 1.97(b) but before the mailing date of either a final action or a notice of allowance.

(1) \_\_\_ The required certification is given below, or

(2) \_\_\_ Enclosed is a check covering the fee set forth in 37 C.F.R. 1.17(p) for consideration of this Statement, or

(3) \_\_\_ Charge the fee set forth in 37 C.F.R. 1.17(p) to Deposit Account No. 20-0668

(e) \_\_\_ After the mailing date of either a final action or a notice of allowance, but before payment of the issue fee. Petition hereby is made for consideration of this Statement and the required certification is indicated below.

(1) \_\_\_ Enclosed is a check covering the fee set forth in 37 C.F.R. 1.17(i)(1), or

(2) \_\_\_ Charge the fee set forth in 37 C.F.R. 1.17(i)(1) to Deposit Account No. 20-0668.

4. Certification (if applicable)


(a) \_\_\_ The undersigned hereby certifies that each item of information contained in this Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than 3 months prior to the filing of this Statement.

(b) \_\_\_ The undersigned hereby certifies that no item of information contained in this Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the undersigned's knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. 1.56(c) more than 3 months prior to the filing of this Statement.

5. The Commissioner is hereby authorized to charge any additional fees or credit any overpayment to Deposit Account No. 20-0668.

Respectfully Submitted,

ESCHWEILER & ASSOCIATES, LLC

By   
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**CERTIFICATE OF MAILING**

I hereby certify that this paper (along with any paper or item referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first-class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date: September 3, 2003

  
Christine Gillroy

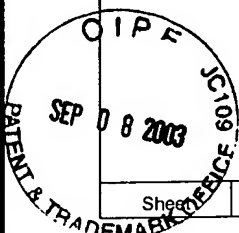
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# **INFORMATION DISCLOSURE STATEMENT BY APPLICANT**

(use as many sheets as necessary)

## **Complete If Known**

Application Number	10/620,516
Filing Date	July 16, 2003
First Named Inventor	Udayakumar et al.
Group Art Unit	
Examiner Name	
Attorney Docket No.	TI-35996

Sheet

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of

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## **U.S. PATENT DOCUMENTS**

Exam. Initials*	Cite No. <sup>1</sup>	U.S. Patent Document		Name of Patentee or Applicant of Cited Doc.	Date of Pub. of Cited Doc. (mm-dd-yyyy)	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code <sup>2</sup> (if known)			
	AA	6,144,060		Park et al.	11/07/2000	Entire Document
	AB	6,225,656	B1	Cuchiario et al.	05/01/2001	Entire Document
	AC					
	AD					
	AF					
	AG					
	AH					

## **FOREIGN PATENT DOCUMENTS**

Exam. Initials*	Cite No. <sup>1</sup>	Foreign Patent Document			Name of Patentee or Applicant of Cited Doc.	Date of Pub. of Cited Doc. (mm-dd-yyyy)	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>5</sup>
		Office <sup>3</sup>	Number <sup>4</sup>	Kind Code <sup>2</sup> (if known)				
	BA							
	BB							
	BF							
	BG							
	BH							

## **OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS**

Exam. Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
	CA	Notes taken at the International Symposium on Applications of Ferroelectrics Conference in Nara, Japan in May, 2002. The speaker was H. Nagel of Infineon Technologies and Toshiba Corporation, Key Technologies for High Density FeRAM Application, one page.	
	CB		
	CC		
	CD		
	CE		
	CF		
	CG		
	CH		

Examiner Signature	Date Considered
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\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

**US and Foreign Patent Documents:** <sup>1</sup>Unique citation designation number. <sup>2</sup>See attached Kinds of U.S. Patent Documents. <sup>3</sup>Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). <sup>4</sup>For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. <sup>5</sup>Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. <sup>6</sup>Applicant is to place a check mark here if English language Translation is attached.

**Other Prior Art/Non-Patent Literature Documents:** <sup>1</sup>Unique citation designation number. <sup>2</sup>Applicant is to place a check mark here if English Translation is attached.

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Notes taken at the International Symposium on Applications of Ferroelectrics Conference in Nara, Japan. The Speaker was H. Nagel of Infineon Technologies and Toshiba Corporation, Key Technologies for High Density FeRAM Application on May, 2002.

He gave a general overview of the status of integration issues with no stress on PZT or SBT talking about issues like deposition temperature, polarization, H<sub>2</sub> barriers. They are using W plugs and vias. Comments on H<sub>2</sub> diffusion barriers:

LPCVD SiN is a good diffusion barrier, but capacitors got damaged during deposition. They used a SiO<sub>2</sub> buffer layer prior to SiN deposition, which solved their problem. He did not answer how thick SiO<sub>2</sub> films were used. Other barriers used in the field include Al<sub>2</sub>O<sub>3</sub>, SiON, TiO<sub>2</sub>/SiO<sub>2</sub>. He ended with some data on 8Mb arrays - Chip size < 76mm<sup>2</sup>;

CMOS: 0.25  $\mu\text{m}$ ; Capacitor area 0.9x0.95  $\mu\text{m}$ ; cell area 5.1  $\mu\text{m}^2$ ; chain cell structure. He showed bit distribution using PZT films with a separation of 1.03V; no fatigue up to 10<sup>11</sup> cycles as measured by amp signal, zeros at 1600 mV and ones at 2600 mV.